REMARKS

This Amendment is submitted under Rule 115 (37 C.F.R. § 1.115). The following remarks are included in accordance with Rule 111 (37 C.F.R. § 1.111).

Claims 14-17, 21, 22, 24, 38-41, 45, 46, and 48 have been cancelled. Claims 7, 12, 13, 31, and 37 have been amended as shown by the clean version appearing above and the marked-up version attached hereto as "**Version with markings to show changes made**". The amendments to these claims provide compliance with requirements regarding provision of proper antecedent bases and improve the form of the claims. The claims as amended by the Amendment are deemed to be allowable. A notice of allowance is earnestly solicited.

Respectfully submitted,

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Version with markings to show changes made

In the following, the markings indicate as follows:

Delete language that appears between brackets ("[ ]").

Insert language that is underlined ("__").

IN THE SPECIFICATION:

SYSTEM FOR CONVERTING HARDWARE DESIGNS IN HIGH-LEVEL PROGRAMMING LANGUAGES TO HARDWARE IMPLEMENTATIONS

Cross-Reference to Microfiche Appendix

Appendix A, which is a part of the disclosure in parent U.S. Patent Application Serial No. 08/931,148 filed on September 16, 1997 and which is incorporated herein in its entirety by this reference [present disclosure], is a microfiche appendix consisting of two sheets of microfiche having a total of 176 frames. Microfiche Appendix A is a source code listing of a portion of the code comprising one embodiment of a system for converting hardware designs in a high-level programming language (ANSI C) into a register transfer level hardware description language (Verilog), which is described in more detail below.

Field of the Invention

This invention relates to configuring digital circuits, especially computationally intensive

digital circuitry, such as field programmable gate arrays (FPGAs) and other programmable logic hardware and application specific integrated circuits (ASICs), and, more particularly, to computer aided design of such computationally intensive digital circuitry. Specifically, one embodiment of the invention provides a system for converting

IN THE CLAIMS:

7. (AMENDED) The method of claim 1 wherein the step of compiling comprises the steps of:

mapping predetermined C-type programming language expressions to functionally equivalent HDL program language expressions; and

assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design; and further comprising the step of:

configuring in the HDL synthesizable design an interface for a [the] gate-level hardware representation.

12. (AMEMDED) The method of claim 7, wherein the step of compiling further comprises [comprising] the step of compiling C-type programming language structure assignment, structure function parameters, and structure function return values into HDL synthesizable expressions.

13. (AMENDED) The method of claim 1 wherein the step of compiling comprises the steps of:

compiling a C-type program control flow into an HDL state machine; and

assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design; and further comprising the step of:

configuring in the HDL synthesizable design an interface for a [the] gate-level hardware representation.

31. (AMENDED) The method of claim 25 wherein the step of compiling comprises the steps of:

mapping predetermined C-type programming language expressions to functionally equivalent HDL program language expressions; and

assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design; and further comprising the step of:

configuring in the HDL synthesizable design an interface for a [the] gate-level hardware representation.

37. (AMENDED) The method of claim 25 wherein the step of compiling comprises the steps of:

compiling a C-type program control flow into an HDL state machine; and

assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design; and further comprising the step of:

configuring in the HDL synthesizable design an interface for a [the] gate-level hardware representation.